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On-chip **transient current** monitor for **testing** of low-voltage CMOS IC

V Stopjaková, H Manhaeve, M ... - ..., automation and test in ..., 1999 - portal.acm.org

... due to the fact that these failures may prevent changes of the quiescent **power supply current**[5]-[6]. Therefore, the **transient power supply current testing** (I DDT **testing**) [7]- [8] can beconveniently used to augment the existing **test** methods and to enhance the defect coverage. ...Cited by 23 - Related articles - All 5 versionsFault detection and input stimulus determination for the **testing** of analog integrated circuits based on **power-supply current** monitoring

G Gielen, Z Wang, W Sansen - Proceedings of the 1994 IEEE/ACM ..., 1994 - portal.acm.org

... all attempts of input signal selection, and a compu- tationally expensive **transient** circuit simulation ...A large number of circuits under **testing**, including both the fault-free and the ... Measurements areobtained from the simulated **power-supply current** followed by a discrete frequency ...Cited by 51 - Related articles - BL Direct - All 5 versions[CITATION] I DD pulse response **testing** on analog and digital CMOS circuits

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GH Weiss, DE Young - Electrical Overstress/Electrostatic Discharge ..., 1995

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DK Su, MJ Loinaz, S Masui, BA Wooley - IEEE Journal of Solid-State Circuits, 1993

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... frequency of VRM and several bulk capacitors, b) time response of same PDS to **current transient**,  
 c) 20 amp **current** transients at ... An HP4291 is used to measure capacitor ESR by soldering it to  
 an SMA connector and attaching it to a **test** head through an APC-7 connector. ...

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J Plusquellic, D Chiarulli, S Levitan - International Test Conference, 1996 - CiteSeer

... 1.0 Introduction **Transient** Signal Analysis (TSA) is a new parametric **testing** method for digital  
 integrated circuits. In TSA, tran- sients in both the voltage waveforms at selected **test** points as  
 well as **current** transients on the **power supply** are ana- lyzed to determine the presence ...

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JM Soden, CF Hawkins, RK Gulati, W Mao - Journal of Electronic Testing, 1992 - Springer

... All CMOS circuits have a relatively large **transient current** associated with switching of the logic  
 gates. ... I/O pins generally presents a noisier envi- ronment requiring a slower **test** rate. Tester **current**  
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[Cited by 144](#) - [Related articles](#)Dynamic **power supply current testing** of CMOS SRAMs


J Liu, RZ Makki, A Kayssi - Journal of Electronic Testing, 2000 - Springer

... use of the dy- namic **power supply current**, i DDT , for **testing** SRAMs ... Any time a cell switches  
 states, a measurable dynamic **power supply current** is estab- lished as a result of the induced te  
 mporary path between ... switching of a cell will result in an unexpected **transient current** level in ...

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... to reduce transfer of charge that results deviations in the **power supply** during **transient** states  
 of ... BIC monitor was originally supposed to be used for on-chip **supply current** monitoring, the ... it  
 also in off-chip applications accepting the proper accuracy and **testing** speed degradation ...

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... to validate the idea of a "test suite" where a number of different fault coverages, for different fault types, are ... We use the transient power supply current as indicative of such switching. The iDDT test approach is not meant to compete or replace other test methods, but is meant to ...

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... on the parameters of the kth type of faulty circuit, transient simulation and ... B. Bannister, "Can supply current monitoring be applied to the testing of analog as ... [3] D. Papakostas, A. Hatzopoulos, "Analogue fault identification based on power supply current spectrum," *Electronics ...*

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... It has also been addressed, in part, by attempting the detection of the transient (dynamic) component, /dd, of the power supply current using off-chip sensors [13].

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... All CMOS circuits have a relatively large **transient current** associated with switching of the logic gates. ... I/O pins generally presents a noisier environment requiring a slower **test** rate. Tester **current** leakage presents a similar logic state dependent noise to the VDD pin of the IC. ...

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... are based on the analysis of a circuit's parametric properties, for example, propagation delay, magnitude of **supply current** or **transient** response ... for generating logic tests have been improved over time to handle more types of **fault** behaviors, parametric **testing** strategies offer ...

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## Dynamic power supply current testing of CMOS SRAMs

J. Liu, R.Z. Makki, A. Kayssi - Journal of Electronic Testing, 2000 - Springer

... Erroneous switching of a cell will result in an unexpected **transient current** level in the **power supply**. The detection of this unexpected level of **current** pulse can then be used to infer a defect.

The iDDT **test** method was shown to detect all disturb **faults**, including read-destruct ...

Cited by 12 - Related articles - BL Direct - All 12 versions

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NK Jha, S Kundu - 1990 - Kluwer Academic Pub

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... Note that the defect-free responses in Figures 4 and 6 are different because a different **test pattern** was used in each case. ... in the FCMOS circuit also have a similar iDDT (recall that iDDT is directly computed from the **transient** portion of the AVDD waveform) **current** response. ...

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... It has also been addressed, in part, by attempting the detection of the **transient** (dynamic) component, /dd, of the **power supply current** using off-chip ... Application of the simple **test pattern** that is traditionally used to detect CSAFs will also yield, as a by-product, **fault** ...

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JM Soden, CF Hawkins, RK Gulati, W Mao - Journal of Electronic Testing, 1992 - Springer

... A methodology for obtain- ing Selective IDD a **test patterns** was first proposed by Mat et al. [16]. ... All CMOS circuits have a relatively large **transient current** associated with switching of the logic gates. ... if the output pins are physically disconnected or tri-stated during the **test** and if ...

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... IDDO (ZLs) tests measure the quiescent  $V_{DD}$  (Ys) **power supply current** of the IC [21]. ... The Z, pseudo stuck-at-fault (PSAF) **test** applies a SAF **vector pattern** to the input nodes of each logic gate, but only propagates the signal to that gate's output node [42, 471. ...

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KT Cheng, S Dey, M Rodgers, K Roy - Design Automation Conference, 2000 - Citeseer

... This technique uses a Genetic Algorithm-based approach to generate **patterns** that maximize the ... IC's maximum operating frequency ( $F_{max}$ ) to establish a multi-parameter **test** technique for ... intrinsic and extrinsic (defect) leakages in IC's with high background stand-by **current**. ...

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**IDDT testing versus IDDQ testing**

Y Min, Z Li - Journal of Electronic Testing, 1998 - Springer

... where  $\delta$  shows the variation times of average **transient current** between the **fault-free** and faulty circuits ... The IDDT **test** generation is to find a **test vector** pair to maximize the value of given by (6) for ... resolution limit, the **fault** is IDDT testable, and  $\{v_1, v_2\}$  is then the **test pattern** pair to ...

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### Monitoring power dissipation for fault detection

... tor. In [3] the shape of the **transient** response is used as a guide to **fault** detection.

The ... speed. This will increase **test** time markedly. The **fault** coverage is determined by the minimum observable deviation in the **supply current**. This ...

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... This requires, in part, the use of **fault** isolation circuitry for each pseudo-partition (see Section 4.2). ... This algorithm includes the following two steps. Step 1. In this step the **test** vectors are generated. ... Page 9. **Transient Power Supply Current Monitoring** 31 ...

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... 9;, Repeat fix different I types of faulty circuit Sampling on the parameters of the kth type of faulty circuit, **transient** simulation and discrete frequency crans formation to obtain 9'(.). qpl, ) ... 9, ...

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... **supply current** of the IC [21]. ... Many companies perform some form of I<sub>DDQ</sub> testing, such as **power** down tests, with a small set of test patterns (vectors ... The Z<sub>DDQ</sub> pseudo stuck-at-fault (PSAF) **test** applies a SAF **vector pattern** to the input nodes of each logic gate, but only propagates the ...

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ST Su, RZ Makki - Journal of Electronic Testing, 1992 - Springer

... of the logic state of a memory cell results in a **transient current** pulse in the ... Keywords:Current-testable design, dynamic current monitors, dynamic **power supply** current, **fault** modeling,**pattern** sensitivity. ... there have been a number of studies aimed at reducing the **test** length [2]-[9] ...[Cited by 35](#) - [Related articles](#) - [All 2 versions](#)**[CITATION]** Defect detection with **transient current** testing and its potentialfor deep sub-micron CMOS ICsM Sachdev, P Janssen, V Zieren - **Test** Conference, 1998. Proceedings., ..., 1998[Cited by 71](#) - [Related articles](#) - [All 2 versions](#)**[CITATION]** A **test pattern** generation methodology for low **power** consumption[psu.edu](#) [PDF]E Corno, P Pinetto, M Rebaudengo, MS Reorda, DA e ... - 16th IEEE VLSI **Test** ..., 1998[Cited by 65](#) - [Related articles](#) - [All 6 versions](#)**[CITATION]** Process-tolerant **test** with energy consumption ratioB Vinnakota, W Jiang, D Sun - **Test** Conference, 1998. Proceedings., International, 1998[Cited by 35](#) - [Related articles](#) - [All 2 versions](#)**[CITATION]** I DD pulse response testing on analog and digital CMOScircuitsJS Beasley, H Ramamurthy, J Ramirez-Angulo, M ... - **Test** Conference, 1993. ..., 1993[Cited by 53](#) - [Related articles](#) - [BL Direct](#) - [All 2 versions](#)**[CITATION]** A 2-ns detecting time, 2- $\mu$ m CMOS built-in current sensingcircuit

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... All CMOS circuits have a relatively large **transient current** associated with switching of the logic gates. ... I/O pins generally presents a noisier environment requiring a slower **test** rate. ... One proposed design integrates the IDDQ monitor into the **power supply** in an attempt to reduce ...

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... Erroneous switching of a cell will result in an unexpected **transient current** level in the **power supply**. ... The iDDT **test** method was shown to detect all disturb **faults**, including read-destruct **faults** using a short **test** length of 5n where n is the number of cells, but this **test** method ...

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... When some inputs change from logic 1(0) to logic 0(1), the **power supply** current ... where  $\delta$  shows the variation times of average **transient current** between the **fault-free** and faulty circuits. ... hardware resolution limit, the **fault** is IDDT testable, and  $\{v_1, v_2\}$  is then the **test pattern** pair to ...

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... is typically on the order of tens of nanoamperes, while the **transient current** may reach ... Therefore, the average **power** dissipation overhead is about 12.4% due to the in ... Future work includes automatic **test** equipment interfacing, **test pattern** generation, and partitioning of large ...

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